



JUNE 23-27, 2024

MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA

Samsung's robust IP QA flow using Solido Crosscheck

Peter Park (Samsung Electronics)

Hyeonyoung Shin (Samsung Electronics)

Siddharth Ravikumar (Siemens EDA)

Seongmin Lee (Siemens EDA)



IP production and integration at Samsung

TEAMS	IPs
Library development	<ul style="list-style-type: none">• Samsung developed IPs - SRAM, IOs and Stdcells, NVM• 3rd party IPs - SRAM, IOs and Stdcells
IP development	<ul style="list-style-type: none">• Samsung developed IPs -Analog and Digital IP• 3rd party IPs- Analog and digital IPs
Foundry Design Service	<ul style="list-style-type: none">• Chip implementation for customer
PDK development	<ul style="list-style-type: none">• PDK(spice, drc, lvs deck development)

IP QA challenges at Samsung

Multiple library IP design kits with different flavours and tech nodes

Samsung's IP designer standpoint:

- Foundation IP should be consistent with the first impression
- Inconsistencies in the Library DK can lead to issues later in the flow

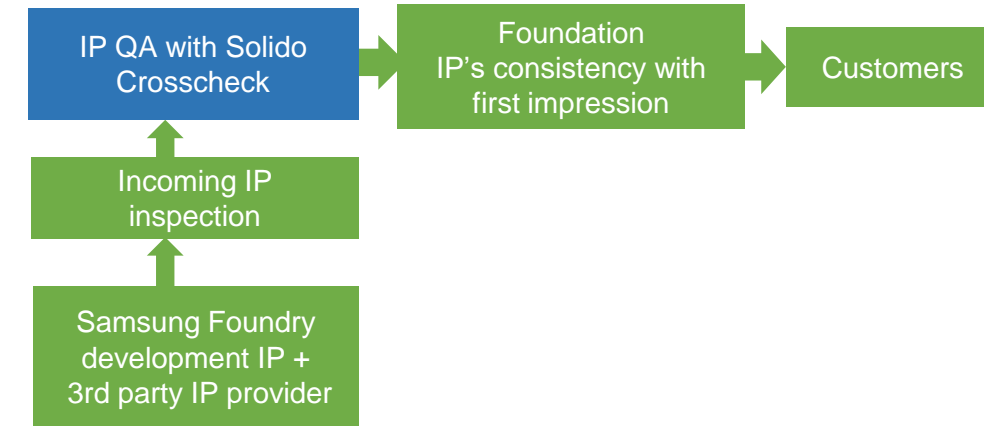
Samsung's IP development standpoint:

- Samsung has several research centres in various countries
- IPs developed in each research centres must have the same quality and do the same QA

Complexity of IP design at smaller tech nodes

- As the file size, number of cells, and number of corners increase, TAT increases
- The complexity of IP designs leads to more new formats, requiring specialized expertise and a steep learning curve
- Systematic QA system ensures the early detection of bugs early in the design flow, contributing to a more efficient and reliable development process

With increasing design IP complexity, QA-approved solutions enhance integration, silicon outcomes, and production schedules



Unit: MB/base kit	14nm	05nm
lib (1file)	72 MB	$\xrightarrow{2.3X}$ 163MB
lib-ccs-tn (1file)	629 MB	$\xrightarrow{2.8X}$ 1799 MB
CELLS		
• Optimize a function combination that is widely used in SOC design as a single cell		
• Providing various drive strengths	809	$\xrightarrow{1.2X}$ 954
• In case of PnR, add various finishing cells for area efficiency		
• DECAP functionality integrated into BUF/INV		
PVTS (general-foundry)	20	$\xrightarrow{1.7X}$ 35

Fig. Increase in file size, number of cells, PVTs with smaller tech nodes

Samsung's IP QA Flow with Siemens' Solido Crosscheck

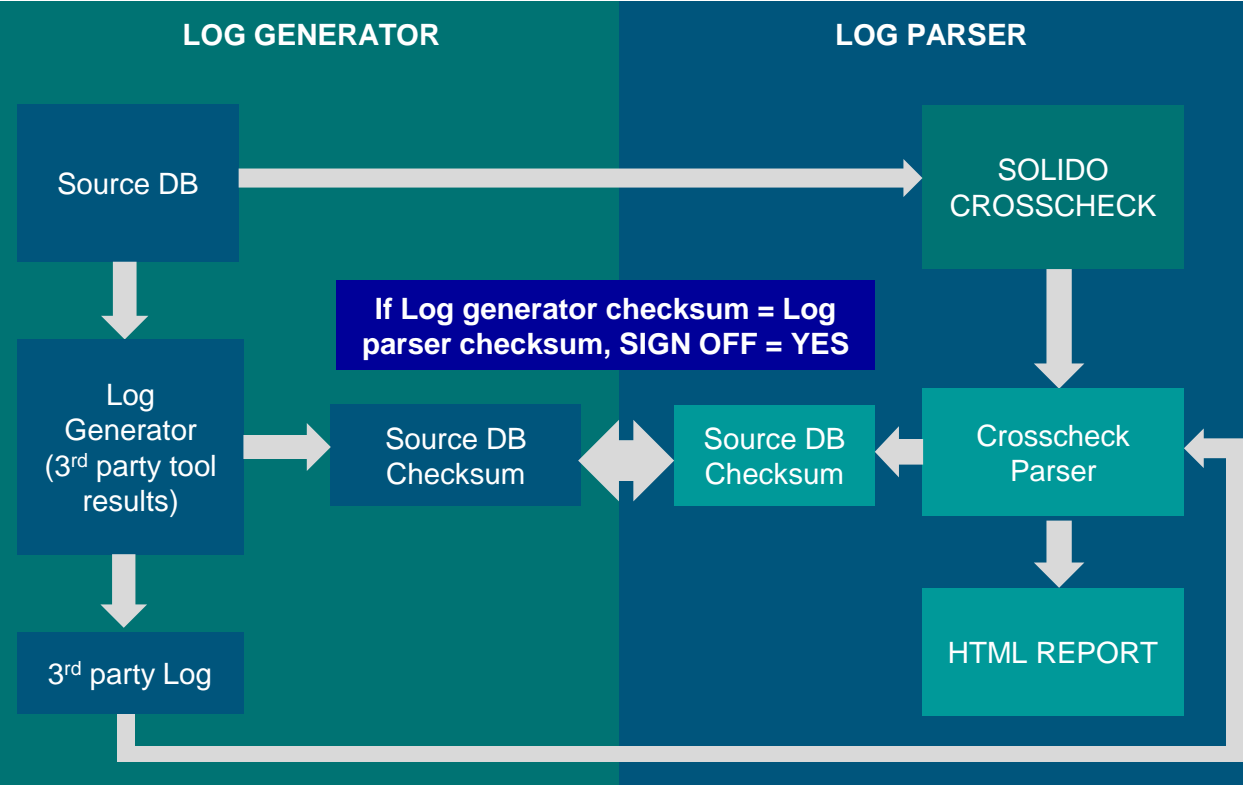
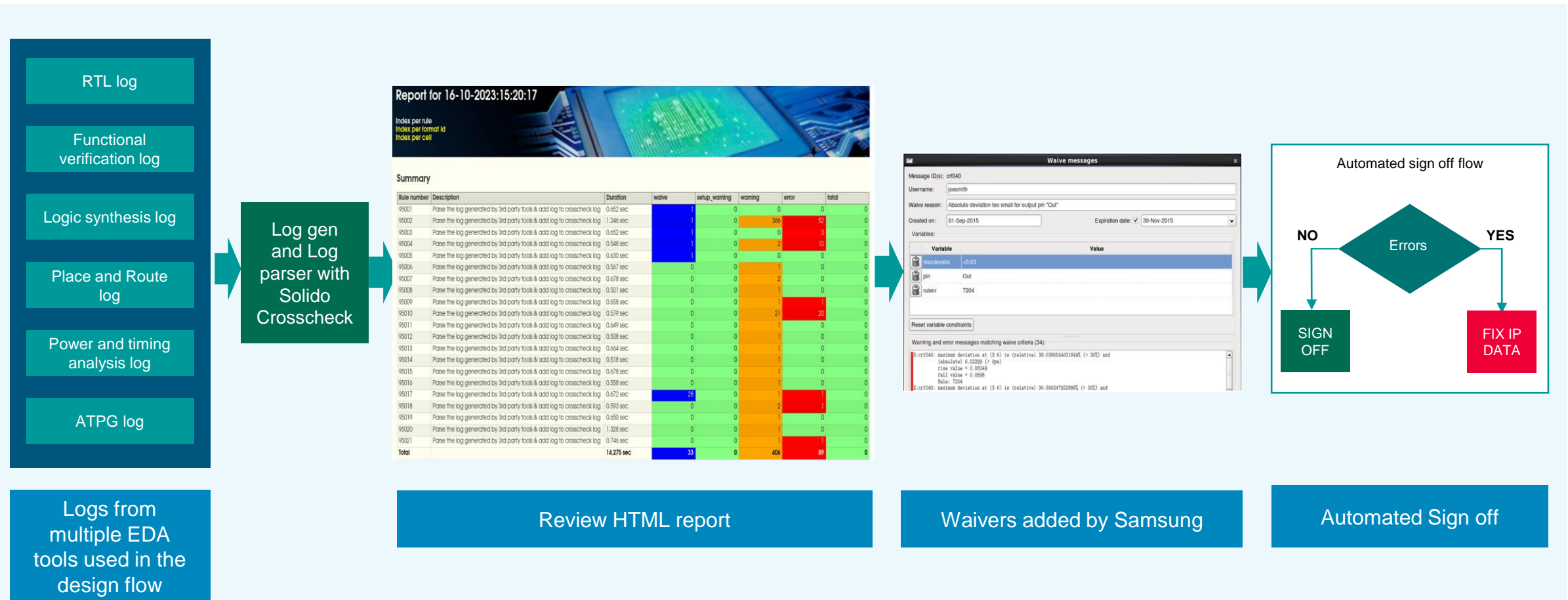


Fig. Samsung's IP QA flow with Solido Crosscheck

Samsung's IP QA flow utilizes Siemens' Crosscheck for automated and comprehensive verification, encompassing Fundamental and Full QA levels to ensure design integrity and reliability

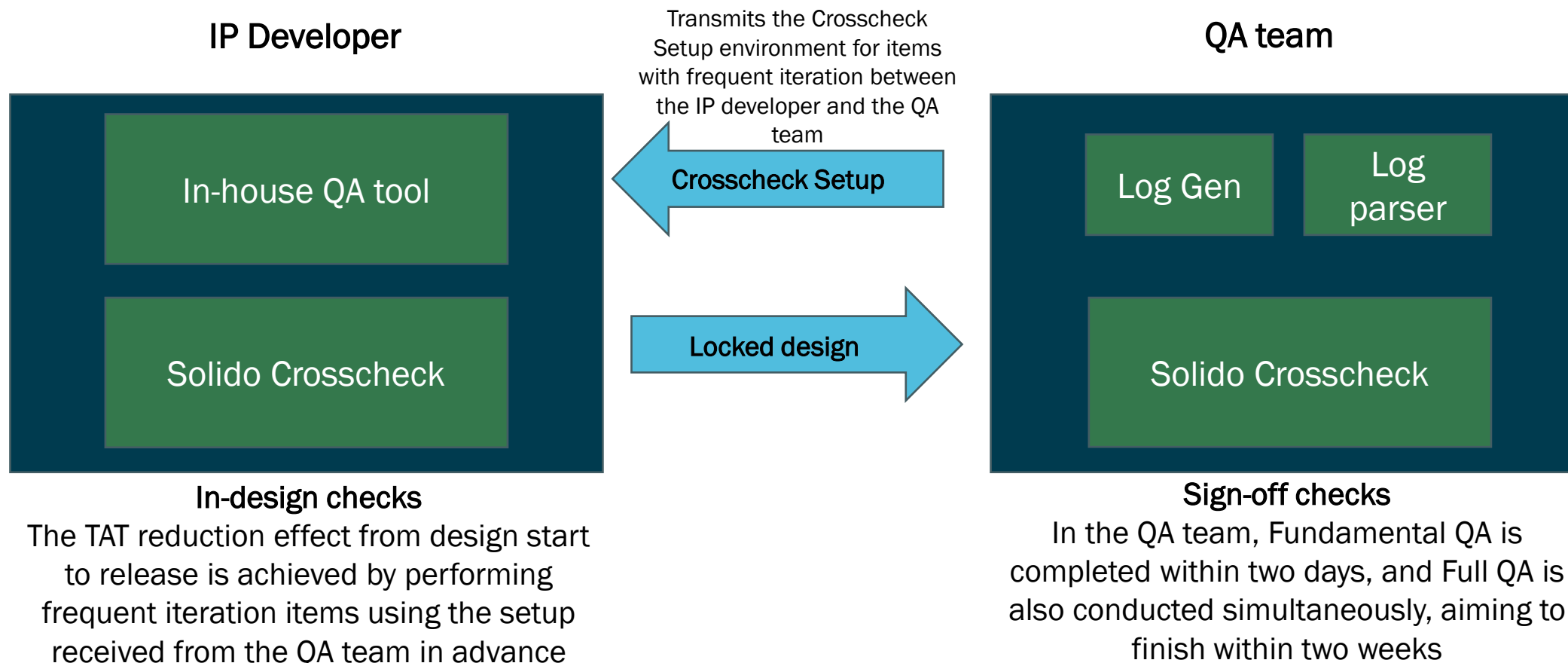
DESIGN LEVEL QA	CELL LEVEL QA
<p>Netlist-based QA: Front-end and back-end (FE/BE) implementation flow checks</p> <p>STD Cell:</p> <ul style="list-style-type: none">• Check if all cells are synthesizable. <p>PMK cell:</p> <ul style="list-style-type: none">• Create power domain with different voltage and check for Liberty property issues. <p>SRAM:</p> <ul style="list-style-type: none">• Wrap SRAM with BIST logic and proceed with FE/BE flow <p>IO:</p> <ul style="list-style-type: none">• Create netlist according to placement guide (map file order)• Perform boundary scan insertion• Execute DRC with random placement	<p>Fundamental QA with significant impact on reliability:</p> <ul style="list-style-type: none">• Cell/port mismatch check: Ensures consistency across views• Design file syntax/format verification: Prevents processing errors• DRC/LVS per cell: Guarantees design rules compliance and layout accuracy <p>Full QA for comprehensive validation:</p> <ul style="list-style-type: none">• Detailed Liberty library value QA: Ensures library accuracy (100+ checks)• Verilog/ATPG/BIST simulation: Verifies functionality and test effectiveness (30+ checks)• Automated Cell Level Full QA:<ul style="list-style-type: none">• Utilizes Crosscheck to manage all QA steps• HTML reports improve communication

Design-Level IP QA



Design-level IP QA ensures that logs from various parts of the design flow are parsed for errors and signed off using a central, unified dashboard

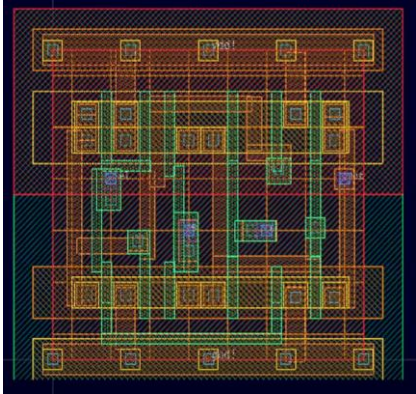
Cell-level IP QA



Items requiring frequent QA and IP developer iterations are automated with Crosscheck, allowing the developer to address issues early and reduce the total turnaround time from design start to release.

Example cell-level fundamental QA checks

Fig. Inconsistencies such as pin name, cell name, and area mismatches between LEF, Verilog, Layout and .libs

LEF	Verilog
<pre>MACRO ADVX2 CLASS CORE ; ORIGIN 0 0 ; ... SIZE 20.0 BY 25.0 ; ... SITE CORE ; PIN D_in DIRECTION INPUT ; PORT LAYER M1 ; RECT 0.1 0.1 0.1 0.1 END END D_in</pre>	<pre>module ADVX_2(D_in, ResetA, ..., CX, VX); input D_in, input ResetA, ... output CX, output VX ... endmodule</pre>
Layout	Liberty
	<pre>cell (ADVX2) { cell_footprint : ADV; area : 30; cell_leakage_power : 0.1; pin (DIN) direction : input; capacitance : 0.05; ... /* .lib table data */ }</pre>

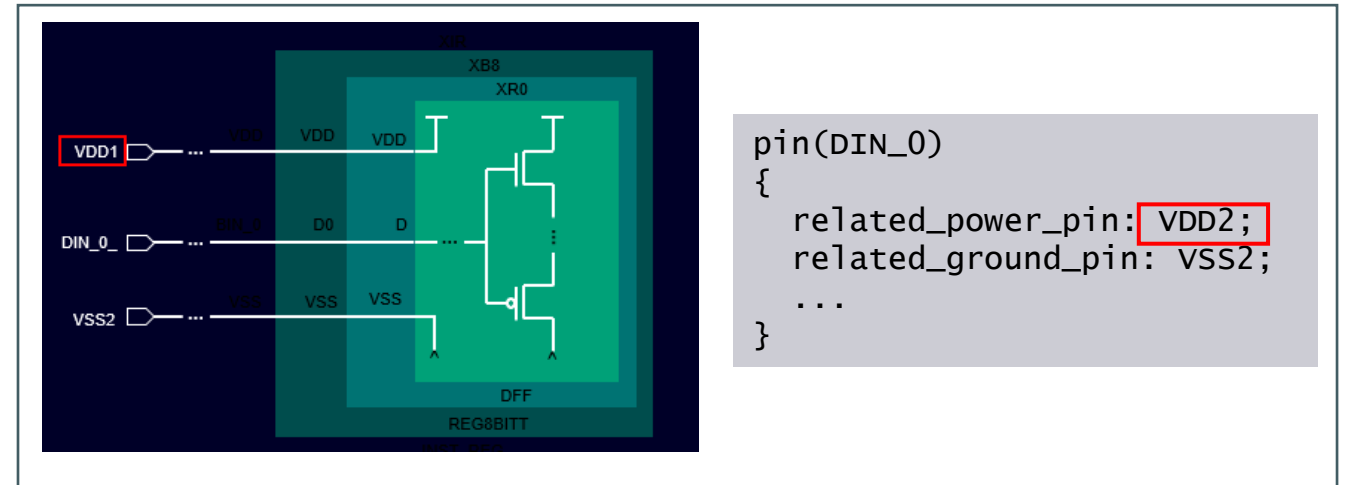
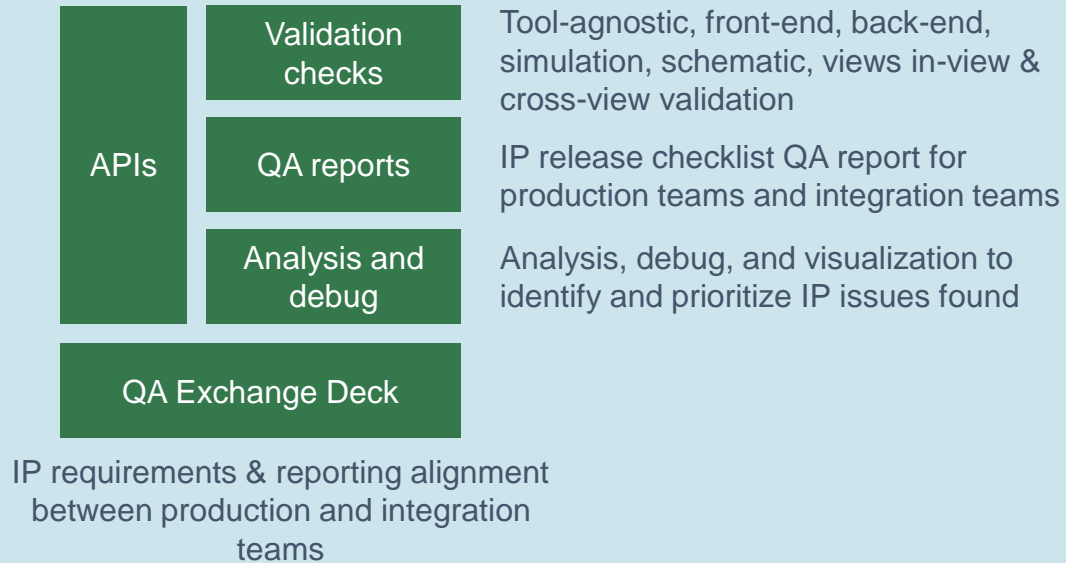


Fig. SPICE netlist and .lib with related power pin connected to the incorrect VDD

It's crucial to perform fundamental QA checks at the cell level early in the design cycle to prevent unexpected issues during the LVS stage

Siemens Solido Crosscheck's approach to IP Validation

Solido Crosscheck IP QA Framework



Cross-view consistency	Library & physical info	Timing, power & noise	Misc.
<ul style="list-style-type: none">• Database consistency<ul style="list-style-type: none">– Naming– Hierarchy– Presence• Terminals• Pins/nets/labels• Timing arcs	<ul style="list-style-type: none">• Cell names• Cell presence• Cell dimension• Functional equivalence• Routability• Abutment• Layout vs. layout	<ul style="list-style-type: none">• Corner vs. corner• NLDM, NLPM• CCS• ECSM• LVF• Electromigration	<ul style="list-style-type: none">• Power Domain• Special Interface• Schematic <p>Custom checks are supported using Crosscheck API</p>

Solido Crosscheck is an IP QA framework for in-view, cross-view consistency checks across all formats, and is independent of IP type or technology

Samsung custom checks and formats using Solido Crosscheck APIs

Crosscheck API

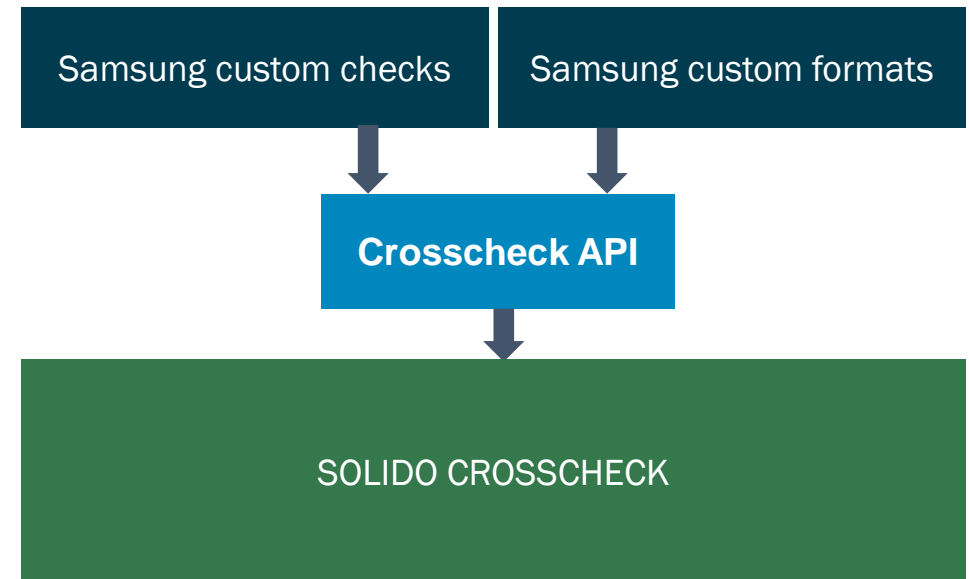
- Create user-defined checks
- Parse in custom formats

APIs are Python-based (V3)

Custom checks at Samsung

- 30+ custom checks developed by Siemens Solido Crosscheck support
- 52 custom checks developed by Samsung Foundry

Fig. Flow extensibility with APIs



Crosscheck's API enables Samsung to enhance existing tool functionalities by adding custom checks and formats

Example custom check: Missing EDA views in IP data

```
variables:
  DESIGN: 'LIB_NAME'
  IPNAME: 'IP'

${IPNAME}1:
  doc:
  file: [.ppt, .pptx, .doc, .pdf]
  lib:
    pattern: CELLNAME_(ffgbc|ssgwc|ttwc)(\d+p\d+v)(m?\d+c)
      PVT
      - ffgbc, 0p99v, 0c
      - ffgbc, 0p99v, 120c
      - ffgbc, 0p99v, m40c

  file: README
```

Simple YAML script to report

- Extra/missing files
- Extra/missing views

Issues at Samsung:

Missing EDA view or Files generated by memory compiler

- Incorrect liberty names
- ECSM, CCS files saved with NLDM extension

Crosscheck integrations with Calibre and Solido Analytics

Fig. Solido Analytics integration

AI outlier detection automatically finds potential issues across PVTs and other parameters in .libs

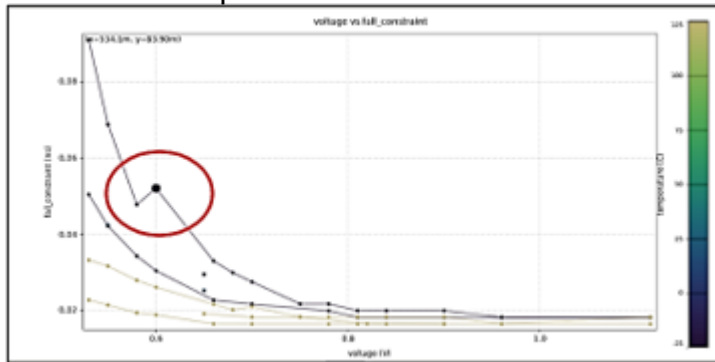
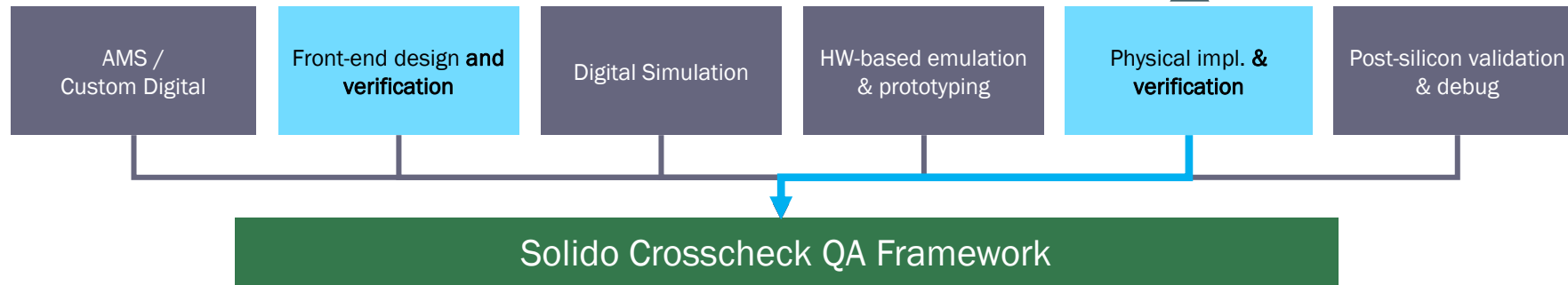
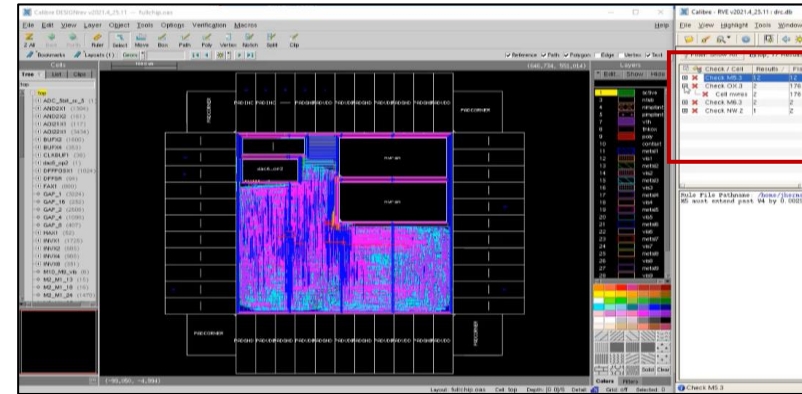


Fig. Calibre DRC integration

layout rule violations such as spacing, width, enclosure, and overlap issues



Seamless integrations with Calibre and Solido Analytics, enables IP production & QA teams to incorporate Calibre and Analytics checks as part of current workflow

Evidence: Results metrics and quality issues prevented by IP QA

Approximately 162 checks enabled

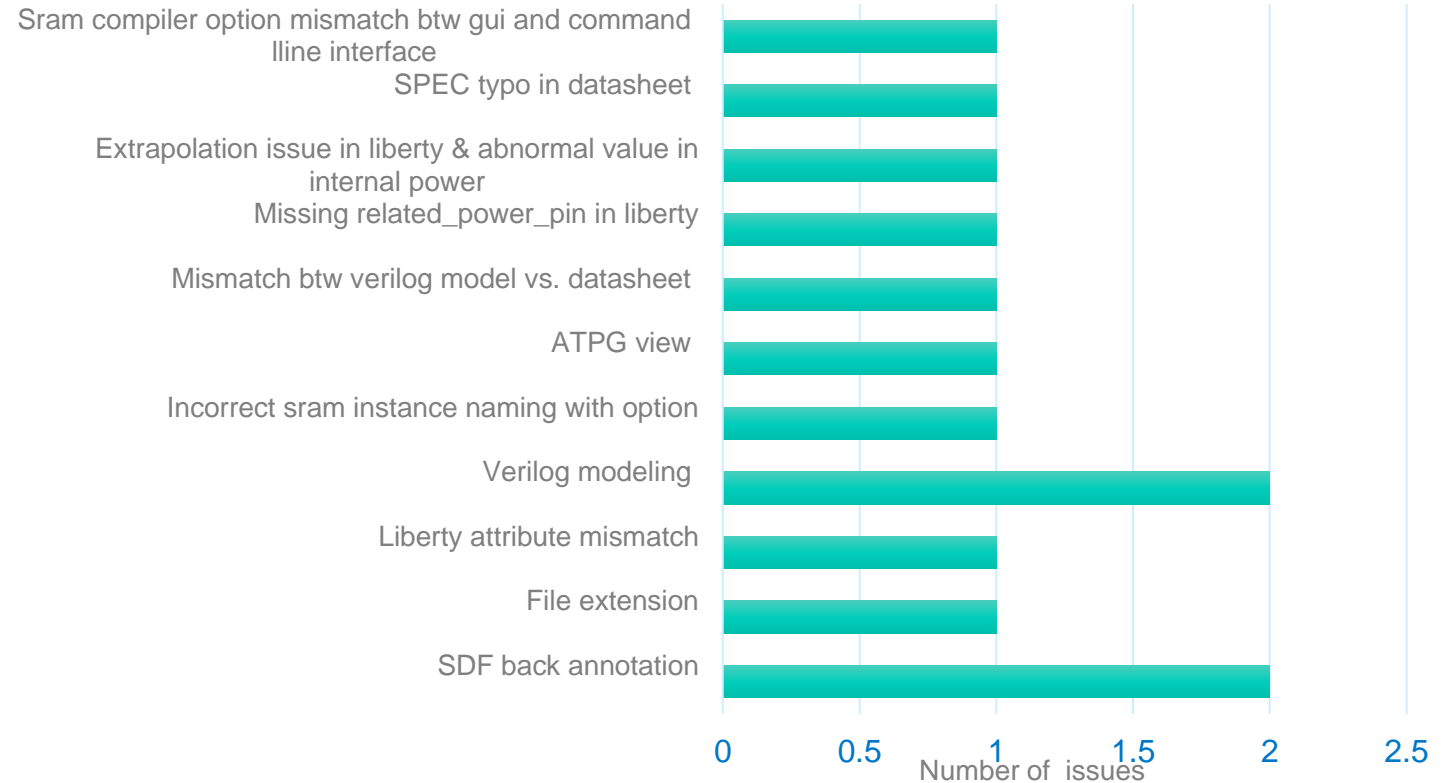
- 82 custom checks + 80 native checks

IP QA performed on over 200 3rd party vendor Library Kits (Std Cells, SRAM, IO)

Types of checks that identified issues



Issues discovered across 5 different tech nodes during an incoming inspection for a 3rd party memory compiler



Benefit: Standardized solution streamlines Samsung's IP QA for efficient, accurate results across all IPs

Summary

IP QA is a key step to successful silicon both for production and integration teams

- Robust IP QA results in better silicon quality and shorter production schedules

Samsung's flow + Solido Crosscheck

- Samsung's IP QA flow utilizes Siemens' Crosscheck for automated and comprehensive verification, encompassing Fundamental and Full QA levels to ensure design integrity and reliability
- Solido Crosscheck includes 300+ native checks, reporting, waiving, and visualization
- Samsung enables custom checks and formats using Crosscheck API extensibility

Automated sign-off flow

- Highly scalable and efficient flow that reduces time and engineering effort

Samsung's robust IP QA methodology, using Solido Crosscheck, accelerates IP production cycles, design tape-out schedules, and enhances the final quality of silicon